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Field-Effect Transistor Figures of Merit for VLS-Grown Ge1-xSnx (x = 0.03-0.09) Nanowire Devices

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KEYWORDS - $Ge_{1-x}Sn_x$ nanowires, low temperature processing, contact resistance, carrier mobility, subthreshold slope, MOSFETs.

ABSTRACT

$Ge_{1-x}Sn_x$ alloys form a heterogeneous material system with high potential application in both optoelectronic and high speed electronics devices. The attractiveness of $Ge_{1-x}Sn_x$ lies in the ability to tune the semiconductor bandgap and electronic properties as a function of Sn concentration. Advances in $Ge_{1-x}Sn_x$ material synthesis have raised expectations recently, but there are considerable problems in terms of device demonstration. Although $Ge_{1-x}Sn_x$ thin films have been previously experimentally explored, in-depth studies of the electrical properties of $Ge_{1-x}Sn_x$ nanostructures are very limited, specifically nanowires grown via a bottom-up vapor-liquid-solid (VLS) process using metal catalysts. In this study a detailed electrical investigation is presented of nominally undoped $Ge_{1-x}Sn_x$ bottom-up-grown nanowire devices with different Sn percentages (3-9 at.%). The entire device fabrication process is performed at relatively low temperatures, the maximum temperature being 440 °C. Device current modulation is performed through backgating from a substrate electrode achieving impressive on-off current (I_{ON}/I_{OFF}) ratios of up to 10^5, showing their potential for electronic and sensor-based applications. Through an extensive parameter extraction routine it is clear that contact resistance (R_C) extraction is essential for proper VLS-grown nanowire device electrical evaluation. Once the R_C contribution is extracted and removed, parameter values such as mobility, can change significantly, by up to 70 % in this work. When benchmarked against other $Ge_{1-x}Sn_x$ electron devices, the VLS-grown nanowire devices have potential in applications where a high I_{ON}/I_{OFF} ratio is important, and where thermal budget and processing temperatures are required to be kept to a minimum.

I. INTRODUCTION

Recently electronic miniaturization has reached fundamental physical constraints, therefore substantial efforts are being made in defining the performance limits and exploring new applications to overcome this, including the development of devices based on 3D nanostructures [1-3], many fabricated from bottom-up grown nanowires [4]. In recent decades advances in nanowire synthesis and fabrication have led to the development of devices such as field effect transistors [5-6], logic circuits [7], sensing devices [8-9] and solar cells [10]. Nevertheless, despite the great achievements reached with Si [5] continual semiconductor innovation has encouraged the exploration of new frontiers, such as developing III-Vs or other group IV semiconductors nanowires.

Although remarkable results for Ge [11], GaN [12] and InAs [1] have been reported in the literature, nowadays GeSn, a relatively immature group IV semiconductor alloy, appears to be a very attractive material due to its fundamental properties. Several key factors have contributed to the advancement of $Ge_{1-x}Sn_x$, such as the ability to tune its bandgap as a function of Sn concentration [13-14], higher electron and hole mobility compared to Si and Ge [15] and easy integration into the already well-established Si manufacturing technology platforms. $Ge_{1-x}Sn_x$ alloys enable a heterogeneous material system, usable both for optoelectronic purposes, *e.g.* lasers [16-17] and photodetectors [18-19], or for high speed electronics devices [20-21].

Recently, chemically synthesized nanomaterials and bottom-up methodologies have been proposed to sustain the relentless progress in the development of new concepts for future electronics. These procedures may present advantages over the already consolidated top-down lithography process, such as the higher degree of structural and surface perfection even as the gate length is scaled, or the lower manufacturing cost. Specifically in the case of novel alloys such as $Ge_{1-x}Sn_x$, to date, $Ge_{1-x}Sn_x$ nanowires have been developed in two different ways, either by using Ge nanowires as a template material in order to obtain Ge/GeSn anisotropic single

crystalline core-shell nanowires [22], or through metal-seed growth via gas phase [23-25] or solution-based synthesis [26-27].

In parallel, the modelling community have extracted parameters and models for $Ge_{1-x}Sn_x$ of various compositions [28-31], for device design and have provided valuable insights into the physics of this complex alloy system [32-34]. Improving the processing aspects, coupled with simulation analysis might lead to breakthrough results in future for $Ge_{1-x}Sn_x$ nanowires devices.

However, despite the extensive studies and the continuous improvement of $Ge_{1-x}Sn_x$ there are only few reports on the electronic properties of the $Ge_{1-x}Sn_x$ nanostructures [35]. In the context of a bottom-up approach, there are limited reports on the implementation of bottom-up grown nanowires in FET-like devices. Only recently, $Ge_{0.81}Sn_{0.19}$ nanowires were shown to have higher conductivity compared to pure Ge nanowires by fabricating simple two and four terminal devices to individual nanowires [35]. In contrast, top-down fabricated $Ge_{1-x}Sn_x$ nanostructures, based on the etching and doping of thin films, show promise as fin-like FET devices [36-37].

Finally, the lack of literature concerning the electronic characterization of bottom-up grown GeSn nanowires, with different Sn concentrations, prevents us from benchmarking the performance of $Ge_{1-x}Sn_x$ nanostructures in various forms. In this article we report for the first time some of the most important FET electronic figures of merit for nominally undoped, VLS-grown $Ge_{1-x}Sn_x$ nanowires, such as mobility, I_{ON}/I_{OFF} ratio, subthreshold swing (SS) and transconductance (gm) as a function of Sn content (x = 0.03, 0.06 and 0.09).

II. EXPERIMENTAL

A. $Ge_{1-x}Sn_x$ nanowire synthesis

$Ge_{1-x}Sn_x$ nanowires (with x ranging from 0.03 to 0.09) were grown via a liquid-injection chemical vapor deposition (LICVD) technique, as previously described [23-24]. A continuous-flow reaction was adopted for nanowire growth on Si (001) substrates, coated with AuAg (90:10 and 80:20) nanoparticle seeds, in a toluene medium using a LICVD technique. Solutions of diphenylgermane (DPG), the Ge precursor, and different Sn precursors (allyltributylstannane (ATBS) and tetraethyltin (TET)) in anhydrous toluene were injected into the metal reaction cell using a syringe pump at a constant rate of 0.025 ml min^{-1} with a parallel flow of H_2/Ar at a rate of 0.5 sccm. The growth temperature was set at 440 °C. Post-grown nanowires were washed with dry toluene and dried under N_2 flow for further characterization.

B. $Ge_{1-x}Sn_x$ nanowire device processing

A schematic representation of the process flow used to contact $Ge_{1-x}Sn_x$ nanowires is shown in Figure 1. Nanowires with different mean Sn contents ($Ge_{0.97}Sn_{0.03}$, $Ge_{0.94}Sn_{0.06}$, and $Ge_{0.91}Sn_{0.09}$) were transferred onto a highly p-doped Si substrate with a thermally grown SiO_2 layer (250 nm thick) and with predefined macroscopic Ti-Au metal bonding pads. The Si/SiO_2 pre-patterned wafer was cleaned using a dip it for 30 sec in acetone, 30 sec in isopropyl alcohol and subsequently rinsed it under deionised (DI) water for another 30 sec. After the cleaning stage the nanowires were dropped onto the substrate and prior to electron beam lithography (EBL) processing, each sample was analyzed with a scanning electron microscope (SEM), to detect the nanowire spreading density on the wafer surface. After inspection, source-drain (S/D) contacts were fabricated; each sample was covered by a polymethyl methacrylate (PMMA) photoresist layer and subsequently exposed at 10 keV to create patterned structures. Directly after the S/D contacts exposure the samples underwent native oxide removal from the

unmasked surface; they were dipped for 10 sec in a buffered oxide etch (BOE) solution (6 parts 40 % NH_4F and 1 part in 4 of 9 % HF), 30 sec in DI and subsequently dried with a nitrogen gun. Metallisation of the contacts (25 nm of Ni and 35 nm of Au) was deposited in a FC2000 electron beam evaporator at a pressure of 6.6×10^{-5} Pa. Finally, the devices were inspected by SEM and electrical measurements was carried out at room temperature to extract the electrical performance of the $Ge_{1-x}Sn_x$ nanowires.

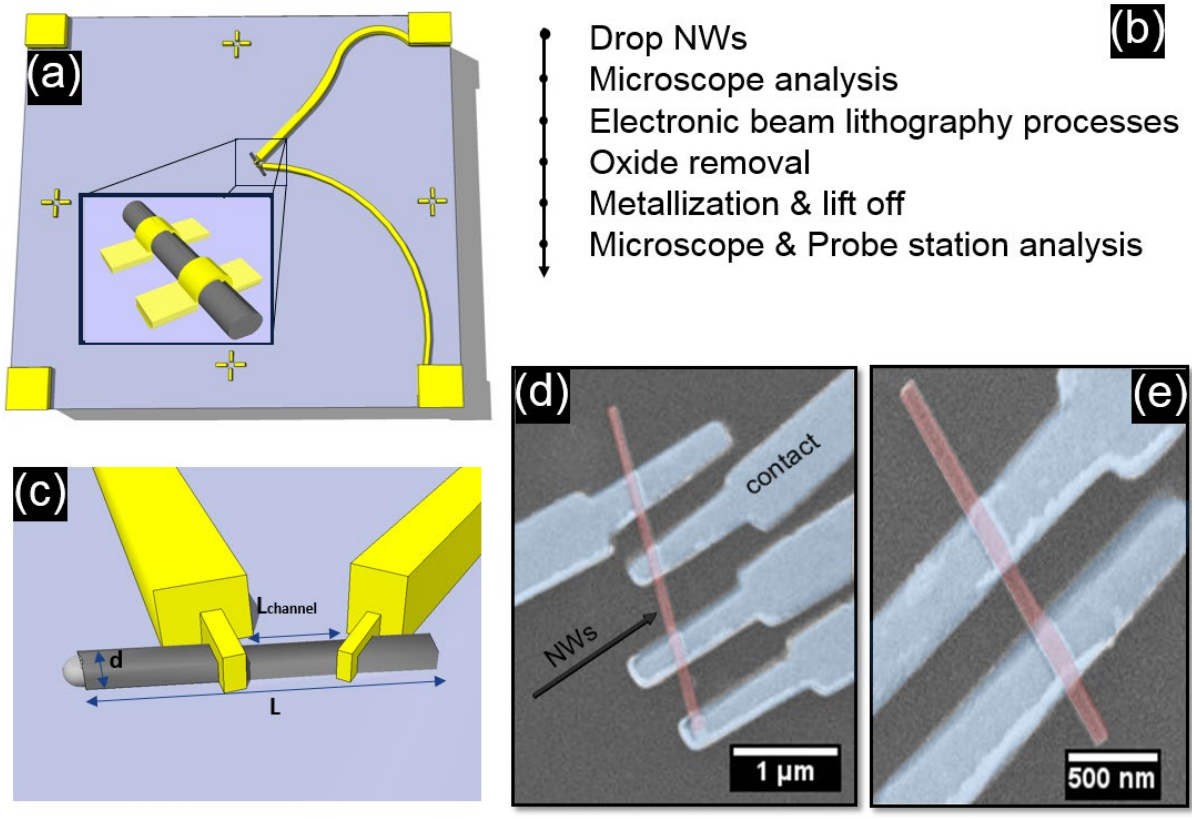

Figure 1: *(a) Illustrative image of the contacting scheme for the bottom-up grown nanowires. (b) A schematic representation of the $Ge_{1-x}Sn_x$ nanowire device process flow used in this study. (c) A close-up schematic and finally (d) and (e) are representative SEM images of $Ge_{1-x}Sn_x$ nanowire device.*

C. $Ge_{1-x}Sn_x$ nanowire device characterisation

Bottom-up grown $Ge_{1-x}Sn_x$ nanowires were imaged on a FEI Helios NanoLab 600i SEM and the devices developed were investigated on the Zeiss Supra55VP SEM. All energy-dispersive X-ray (EDX) measurements for Sn content determination were recorded in high-

angle annular dark-field mode in the FEI Helios NanoLab 600i operating at 30 kV and 0.69 nA with an attached Oxford X-Max 80 detector. The error in the EDX measurements was a standard error of ±0.5 at. %. High-resolution scanning transmission electron microscope (STEM) imaging and electron energy loss spectroscopy (EELS) mapping was performed using a Nion UltraSTEM100 microscope, operated at 100 kV. Electrical measurements at room temperature were carried out with a Cascade semiautomatic prober station and an Agilent (HP) 4156C Parameter Analyser. To minimize the influence of the light the measurements were made in a dark ambient with a detected leakage current in the range of pico Amperes.

III. RESULTS AND DISCUSSION

A. Structural analysis

$Ge_{1-x}Sn_x$ nanowires were synthesized using a VLS procedure employing a gold-silver (AuAg) alloy as metal seeds. Variation of different growth parameters, *e.g.* precursors, temperature, stoichiometry of the AuAg alloy catalyst *etc*., resulted in $Ge_{1-x}Sn_x$ alloy nanowires with different mean Sn contents ranging from 3 - 9 at.%. We have detailed the fabrication process and influence of growth parameters on the morphology, crystal structure and stoichiometry of the $Ge_{1-x}Sn_x$ nanowires in previous publications [23-24]. Most importantly, the morphological quality, *e.g.* uniform diameter, minimal Sn clustering *etc*., of the nanowires was intact for all the three nanowires concentration investigated [38]. An SEM image of $Ge_{1-x}Sn_x$ (x = 0.09) nanowires grown at 440 °C using a $Au_{0.80}Ag_{0.20}$ catalyst and TET as the precursor can be seen in Figure 2(a). Sn incorporation was confirmed via EDX point analysis on the nanowires, which showed a typical standard deviation of 0.6-1.2 at.% from the average Sn content [38]. EDX maps were also generated to confirm the homogenous distribution of Sn in the nanowires, which is crucial to verify the accurate electrical performance of the nanowires (see Figure 2(b)). Determining the structural quality of the $Ge_{1-x}Sn_x$ nanowires is also imperative

for its device implementation. Generally, the crystal structure of the alloy nanowires, with various Sn incorporation, exhibited a 3C lattice arrangement without any stacking faults and twin boundaries. A representative dark field STEM image and corresponding fast Fourier transformation (FFT), shown in Figure 2(c), confirmed the single crystalline nature of the $Ge_{1-x}Sn_x$ (x = 0.09) nanowires with a <111> crystal growth direction.

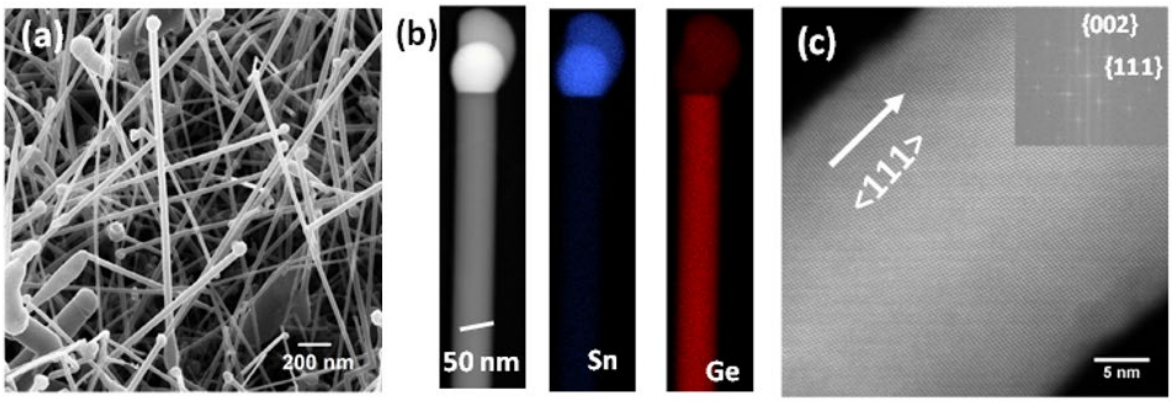

Figure 2: *(a) Representative SEM image of $Ge_{1-x}Sn_x$ (x=0.09) nanowires. (b) EDX mapping and corresponding high-angle annular dark-field (HAADF) image for Ge and Sn in a $Ge_{1-x}Sn_x$ nanowire with 9 at.% of Sn. (c) Lattice-resolved STEM HAADF image recorded from the core of an alloy nanowire showing its single crystalline nature. Corresponding FFT is shown in the inset.*

B. Electrical analysis and parameter extraction

The electrical field effect characteristics of the nominally undoped $Ge_{1-x}Sn_x$ nanowires were determined; thus the transfer characteristics (I_d-V_g) obtained highlight the electrical properties of these nanowires as a function of Sn concentration. Prior to electrical testing nanowire was imaged by SEM to confirm the morphological quality of the devices and to determine the device geometry, *e.g.* channel length and nanowire diameter.

Firstly, each device was analyzed for current conduction using top contacts (see Figure 1) with the backgate electrode set to 0 V. As expected, since the material is unintentionally doped I_{ds}-V_{ds} characteristics with V_{bg} = 0 , show close to linear behavior through the origin, as seen Figure 3. The quasi-linear electrical features from most of the nanowires indicates non-ideal contacts between the electrode and the nanowires, possibly due to the presence of an

oxide layer at the contact point and/or the relatively low dopant concentrations within the nanowires themselves.

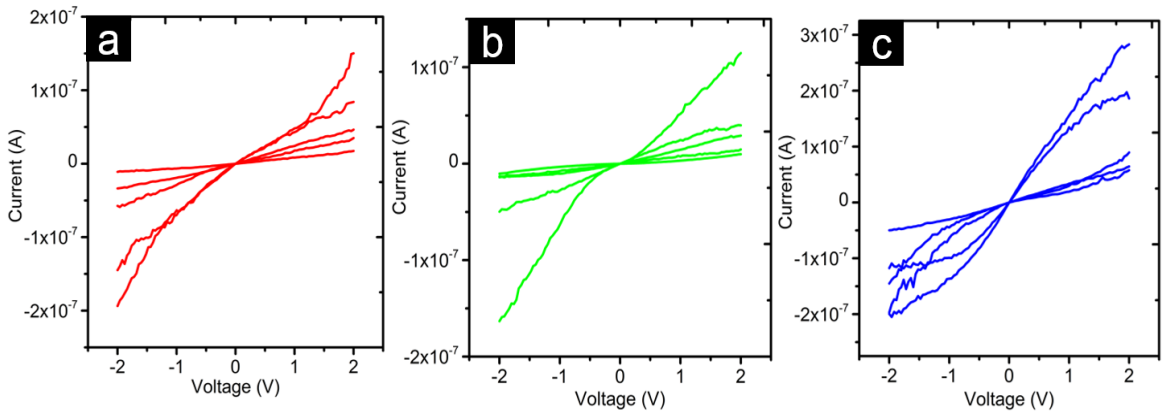

***Figure 3**: Representative I_d-V_d inspection (V_{bg} = 0 V) for the three different nanowire samples; (a) is $Ge_{0.97}Sn_{0.03}$, (b) is $Ge_{0.94}Sn_{0.06}$ (c) $Ge_{0.91}Sn_{0.09}$.*

After the preliminary inspection of the contact behavior, transfer characteristic measurements were performed by sweeping the backgate voltage between -10 V to 10 V and setting the S/D bias voltage as -0.2 or -1 V. The measurement range was carefully selected to prevent damage of nanowires from high current densities and subsequent partial degradation of the devices. Figure 4 shows representative I_{ds}-V_{bg} transfer characteristics of the nanowires as a function of the Sn content and highlights their ability to modulate the current at all Sn concentrations investigated, even without intentional doping. Although the nanowires were nominally undoped, Figure 4 shows that they all display p-type semiconductor features. These characteristics are similar to those previously observed for undoped VLS-grown Ge nanowires, which tend to accumulate holes due to the formation of a negative trapped charge layer at the semiconductor surface [39]. Furthermore, defects in bulk Ge tend to produce p-type charges, for example Romano *et al.* [40] showed that damage from Ge ion implants into Ge created p-type carriers. Even though our nanowires were not ion implanted, intrinsic point defects within the GeSn crystal structures here are likely to be p-type in nature.

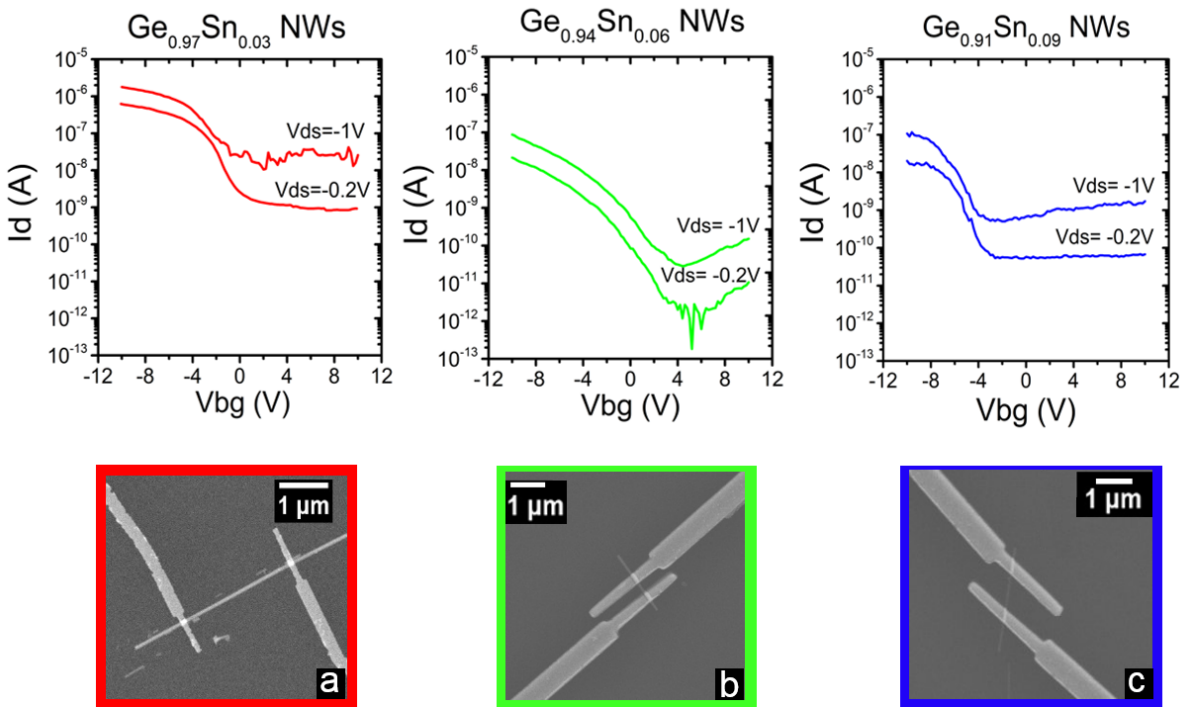

Figure 4: *(Top row) Representative room temperature I_d-V_{bg} characteristics for $Ge_{0.97}Sn_{0.03}$, $Ge_{0.94}Sn_{0.06}$ and $Ge_{0.91}Sn_{0.09}$ nanowires with two different V_d values (-0.2V and -1V). (Bottom row) Representative SEM images of typical nanowire devices with 3, 6, and 9 at.% of Sn in (a), (b), and (c) respectively.*

Extraction of threshold voltages (V_{th}) was carried out using the transconductance derivative methodology at low drain voltages [41]. V_{th} variation as a function of Sn concentration in the nanowire is shown in Figure 5. Mean V_{th} values were calculated in order to compare alloy nanowires with different Sn incorporation. We speculated that the V_{th} variation might derive from the negative surface charge layer given by the GeSn oxides or from the underlying SiO_2 layer. The overlying GeSn oxide layers, being a source of traps, might lead to a more negative flat band potential and consequently to a V_{th} shift (see inset of Figure 5).

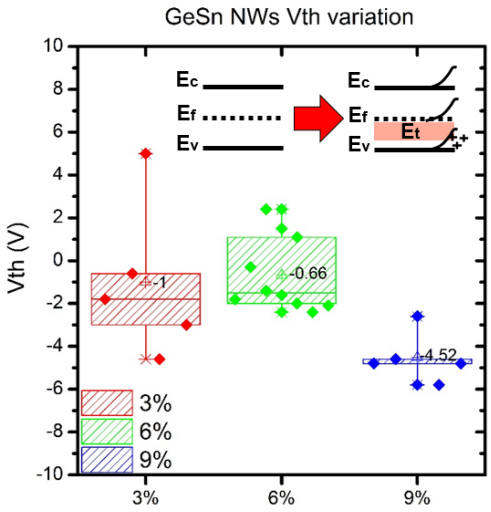

Figure 5: *Box plot for the V_{th} extracted as a function of the Sn % in the $Ge_{1-x}Sn_x$ nanowires. The black text shows the mean number per data set, while all the values measured are presented as scatter points.*

In addition, the I_{ON}/I_{OFF} ratio, sub-threshold slope (SS), and g_m have also been extracted from the electrical characteristics considering 30 % of the V_{gs} swing, below V_{th}, is assigned to the off state while the remaining 70 % is assigned to the on state [1]. Since all of the devices fabricated show very wide variations, as was shown for V_{th} in Figure 5, a mean value has been estimated for each extracted electrical parameter. This methodology allows us to obtain trends based on the Sn concentration, as shown in Figure 6. The highest individual device I_{ON}/I_{OFF} ratio of 10^5 was observed for $Ge_{0.97}Sn_{0.03}$ nanowires, with this ratio decreasing with increasing Sn content; due to the relative increase in I_{OFF} resulting from a reduction in the bandgap of the nanowires.

Concerning SS, values were extracted at the midpoint of the subthreshold characteristic. As expected, using a back-biasing device architecture, the values reported are quite large compared with a typical top-gate biasing FET device. The mean value of the SS varied from 2164 mV/dec, obtained for $Ge_{0.97}Sn_{0.03}$ nanowires, to 1525 mV/dec for $Ge_{0.91}Sn_{0.09}$ nanowires. The minimum SS values obtained for individual nanowires were 1081 mV/dec for $Ge_{0.97}Sn_{0.03}$, 426 mV/dec for $Ge_{0.94}Sn_{0.06}$ and 829 mV/dec for $Ge_{0.91}Sn_{0.09}$ respectively. Despite the

magnitude of the SS variation for each set of nanowires, it was possible to observe a mean decrease in SS with increasing Sn content. Top-gating and a gate-all-around device architecture would be necessary to further reduce these SS values.

Conversely, mean transconductance values ($g_m = \delta_{Id}/\delta_{Vbg}$) decreased with increasing Sn content in the nanowires. The mean value varied between 0.02-0.09 µS with the maximum value of 0.28 µS obtained for $Ge_{0.97}Sn_{0.03}$ nanowires. All of the mean values extracted are summarised in Table 1.

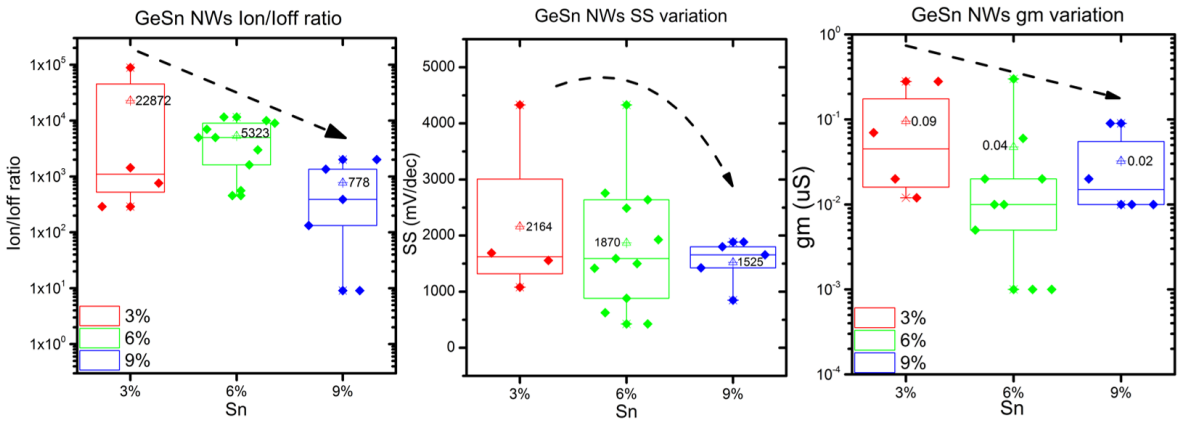

Figure 6: *I_{ON}/I_{OFF}, SS, and g_m extracted from $Ge_{1-x}Sn_x$ nanowire FET devices, as a function of the Sn concentration.*

Table 1: *Summary of the mean values obtained for $Ge_{1-x}Sn_x$ nanowire FET devices as a function of the Sn concentration.*

$Ge_{1-x}Sn_x$ nanowires	Electrical parameters			
	I_{ON}/I_{OFF} ratio	SS (mV/dec)	g_m (µS)	V_{th} (V)
$Ge_{0.97}Sn_{0.03}$	2.28×10^4	2164	0.095	-1
$Ge_{0.94}Sn_{0.06}$	5.32×10^3	1870	0.047	-0.66
$Ge_{0.91}Sn_{0.09}$	7.80×10^2	1525	0.032	-4.52

The trends shown in Figure 6 and in Table 1 can be understood by taking into account gate electrostatic effects. Generally, in a p-type device for $V_g > 0$ holes are depleted from the channel. This effect leads to a decrease in the conductivity while the opposite behavior will happen for $V_g < 0$. However, in our case, since the devices shows p-type behavior, by reducing V_g we observe a remarkable off current increment due to band bending in the channel. The off current increment and the theoretical reduction of the bandgap with increasing Sn content

explains the good electrical performance for the $Ge_{1-x}Sn_x$ nanowires, with a Sn content up to 6 at.%. Beyond 6 at.%, based on our data, the $Ge_{1-x}Sn_x$ alloys become difficult to control, due the small bandgap expected, for electronic applications particularly in a back-gate device architecture, due to the lower electrostatic control compared to a top-gate or gate-all-around architecture.

Figure 7 shows a plot of I_{ON}/I_{OFF} ratios as a function of nanowire width for all three different Sn compositions. There appears to be little or no correlation between I_{ON}/I_{OFF} ratios and nanowire diameter, although the nanowires are relatively large for such a junctionless transistor design. Also the nanowires are undoped, meaning they are likely to be fully depleted when off, and in accumulation when on.

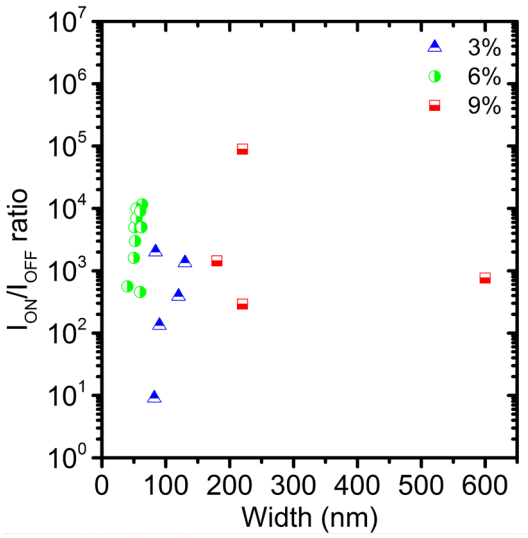

Figure 7: *Scatter plot of I_{ON}/I_{OFF} as a function of nanowire width for the three different Sn compositions.*

Considering the linear region of the I-V curves obtain for the nanowires carrier mobilities were extracted from the transfer characteristics using equation 1:

$$\mu = g_m L/(WCV_{sd}) \qquad (1)$$

where L and W are respectively the nanowire length and width, V_{sd} is the bias between source and drain; C is the capacitance for a backgated nanowire device [6] obtained using equation 2:

$$C = 2\pi\varepsilon\varepsilon_0 L(\cosh^{-1}(\frac{d+2h}{d}))^{-1} \quad (2)$$

with ε as the dielectric constant of the SiO_2 layer of h thickness, and d is nanowire diameter. Taking into consideration nanowire diameters the carrier mobility was extracted for all of the devices using the maximum g_m value. The mean carrier mobility was evaluated for the three different Sn compositions, with values of 2.67, 8.51 and 11.87 cm^2/Vs obtained for $Ge_{0.97}Sn_{0.03}$, $Ge_{0.94}Sn_{0.06}$ and $Ge_{0.91}Sn_{0.09}$ nanowires respectively.

C. Contact resistance evaluation and subsequent parameter extraction

The values obtained using this methodology tend to underestimate V_{th} and carrier mobility due to the non-negligible contribution of the contact resistance. Therefore to take into account the contact resistivity contribution, the Y function method was used [42] to extract both V_{th} and carrier mobility. We utilised the Y function shown in equation 3:

$$Y = \frac{I_{ds}}{gm^{\frac{1}{2}}} = (\frac{W}{L}\mu_0 C_{0x} V_{ds})(V_{gs} - V_{th}) \quad (3)$$

to extract the carrier mobility and the V_{th} from the slope and the intercept of the curve, as shown in Figure 8. In addition, using the Y-function methodology we estimated the contact resistance (R_C) of the backgate MOSFET device using the mobility degradation parameter, shown in equation 4:

$$\theta = \left[\left(\frac{I_{ds}}{g_m(V_{gs} - V_{th})}\right) - 1\right]/(V_{gs} - V_{th}) \quad (4)$$

After extraction, the parameter values were inserted in the following equation $\theta = \theta_0 + R_c C_{ox}\mu_0 \frac{W}{L}$ considering that at large values of V_{gs} ($V_{gs} - V_{th} = 10V$) θ_0 the mobility degradation factor related to the channel scattering is negligible [43] and the major contribution comes from the second term; see Figure 8(a) and (b). Figure 8(c) shows the V_{th} variation after the removal of the R_C contribution. It is possible to see that the V_{th} decreases drastically

compared with previous data in Figure 5 for $Ge_{0.97}Sn_{0.03}$ and $Ge_{0.91}Sn_{0.09}$ nanowires respectively, changing from -1 to -7.25 V and from -4.25 to -9.25 V; while for $Ge_{0.94}Sn_{0.06}$ V_{th} shows a different trend moving from -0.66 to -0.25 V. This highlights the importance of extracting and removing the R_C contribution when estimating electrical parameters from these type of nanowire devices.

Figure 8(d) shows the mobility extracted considering the Y function in equation 3; it is noteworthy that mobility data reported earlier do not take into account the contribution of the contact resistance (2.67 cm^2/Vs for $Ge_{0.97}Sn_{0.03}$, 8.51 cm^2/Vs for $Ge_{0.94}Sn_{0.06}$ and 11.87 cm^2/Vs for $Ge_{0.91}Sn_{0.09}$). With the contribution of R_C accounted for, the μ values become 4.25 cm^2/Vs for $Ge_{0.97}Sn_{0.03}$, 14.54 cm^2/Vs for $Ge_{0.94}Sn_{0.06}$ and 14.80 cm^2/Vs for $Ge_{0.91}Sn_{0.09}$ respectively. Therefore from Figure 8(d) it is evident that for all nanowires the mean carrier mobility increases by 60, 70, and 25 % for $Ge_{0.97}Sn_{0.03}$, $Ge_{0.94}Sn_{0.06}$ and $Ge_{0.91}Sn_{0.09}$ respectively on average, again highlighting the importance of removing the R_C contribution.

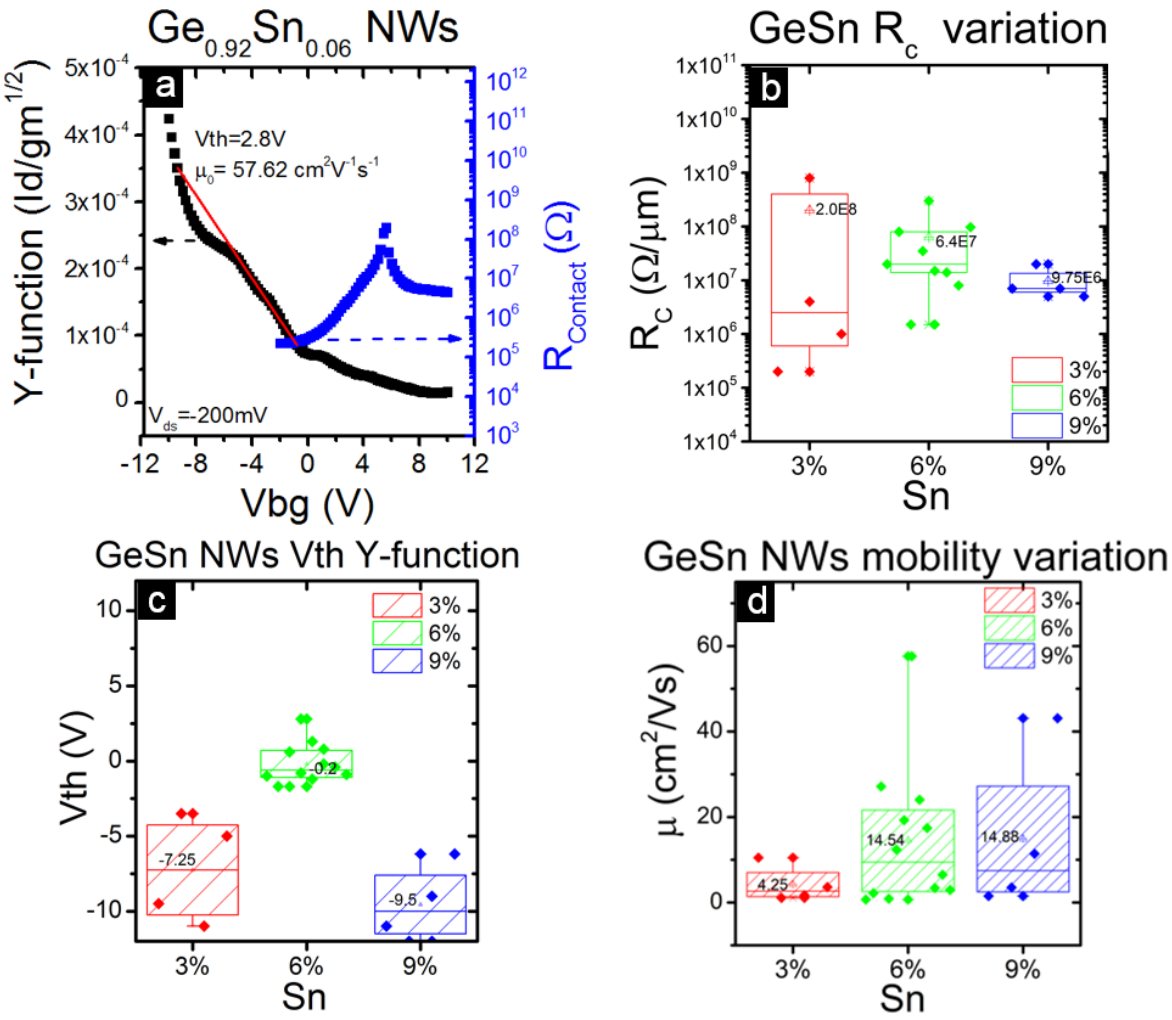

Figure 8: *(a) Y function and contact resistance extraction for a representative 6 at.% Sn nanowire device. (b)* R_C *extracted as a function of the Sn concentration, (c) and (d) show respectively* V_{th} *and mobility trends after the Y function application. In red there are data related to 3 at.% Sn, in green data related to 6 at.% Sn and in blue data related to 9 at.% Sn.*

Data extracted are in accordance with previous results [44], where the carrier mobility increases as a function of the Sn concentration due to the proportional increment of the channel compressive strain which boosts the hole mobility; whilst the major mobility limitations are the phonons and alloy scattering. Note, as expected in a structure like a nanowire, with surfaces on all sides, and consequently enhanced surface carrier scattering, the mobility values are lower than those extracted in thick-films which have minimal surface scattering effects [37, 45-49].

D. Figures of merit comparison for different $Ge_{1-x}Sn_x$ *architectures and devices*

Table 2 and Fig. 9 shows the comparison among the most common electrical parameters obtained to date with different device architectures and GeSn channel compositions considering process temperatures below 1000 °C [48-54].

Table 2: *Electrical parameters comparison for the most important figures of merit extracted from different $Ge_{1-x}Sn_x$ device structures. Data related to this work has been highlighted with red, green and blue as a function of the different Sn concentrations, namely 3, 6, and 9 at.%.*

Year	**2019, this work**			**2019** [50]	**2019** [48]	**2018** [49]	**2017** [52]	**2016** [51]	**2015** [53]	**2014** [54]
Sn%	9	6	3	4	5	5	2	0	2	3
Proc. T.	<440°C	<440°C	<440°C	<300°C	500°C	500°C	>938°C	500°C	>938°C	300°C
Dev. Struc	NWs (bot. gate)	NWs (bot. gate)	NWs (bot. gate)	Planar (top gate)	Planar (top gate)	Planar (bot. gate)	Planar (top gate)	Planar (top gate)	Planar (top gate)	Tri gate
Peak μ	μ=4.25 (cm^2/Vs)	μ=14.54 (cm^2/Vs)	μ=14.9 (cm^2/Vs)	μ=54 (cm^2/Vs)	μ=162 (cm^2/Vs)	μ=39.3 (cm^2/Vs)	μ=26 (cm^2/Vs)	μ=19 (cm^2/Vs)	μ=423 (cm^2/Vs)	μ=31 (cm^2/Vs)
I_{on}/I_{off} ratio	2.3×10^4	5.3×10^3	7.8×10^2	1.2×10^2	2.8×10^5	1.7×10^4	$\approx 10^1$	2×10^3	3×10^2	$\approx 10^5$

Of note, all the documents data shown in Table 2, except for this work, refers to top or bottom gated planar FET devices. Nevertheless, it is possible to see that the data obtained from our study are comparable. Figure 9(a) shows the mobility data obtained as a function of $Ge_{1-x}Sn_x$ channel composition; most of data-points are located between 0 to 50 cm^2/Vs with the exception of [48] and [53] which show mobility values of 162 and 423 cm^2/Vs respectively. Moreover, considering the extreme sensitivity of the material with respect to temperature, Figure 9(b) reports I_{ON}/I_{OFF} ratio as a function of the maximum process temperature used, where it is possible to observe decreasing I_{ON}/I_{OFF} at temperatures approaching 1000 °C. Figure 9(c) shows I_{ON}/I_{OFF} ratio data versus mobility for our nanowires benchmarked against planar structures previously reported in the literature. Figure 9(d) highlights how our VLS-grown nanowires compare with planar device architectures, in terms of I_{ON}/I_{OFF} ratios versus Sn concentration. Overall, considering Sn content, processing temperature and device figures of merit our bottom-up grown $Ge_{1-x}Sn_x$ nanowires have potential in applications where a high on-

to-off current ratio is important, and in particular where the thermal budget and processing temperature are needed to be kept to a minimum.

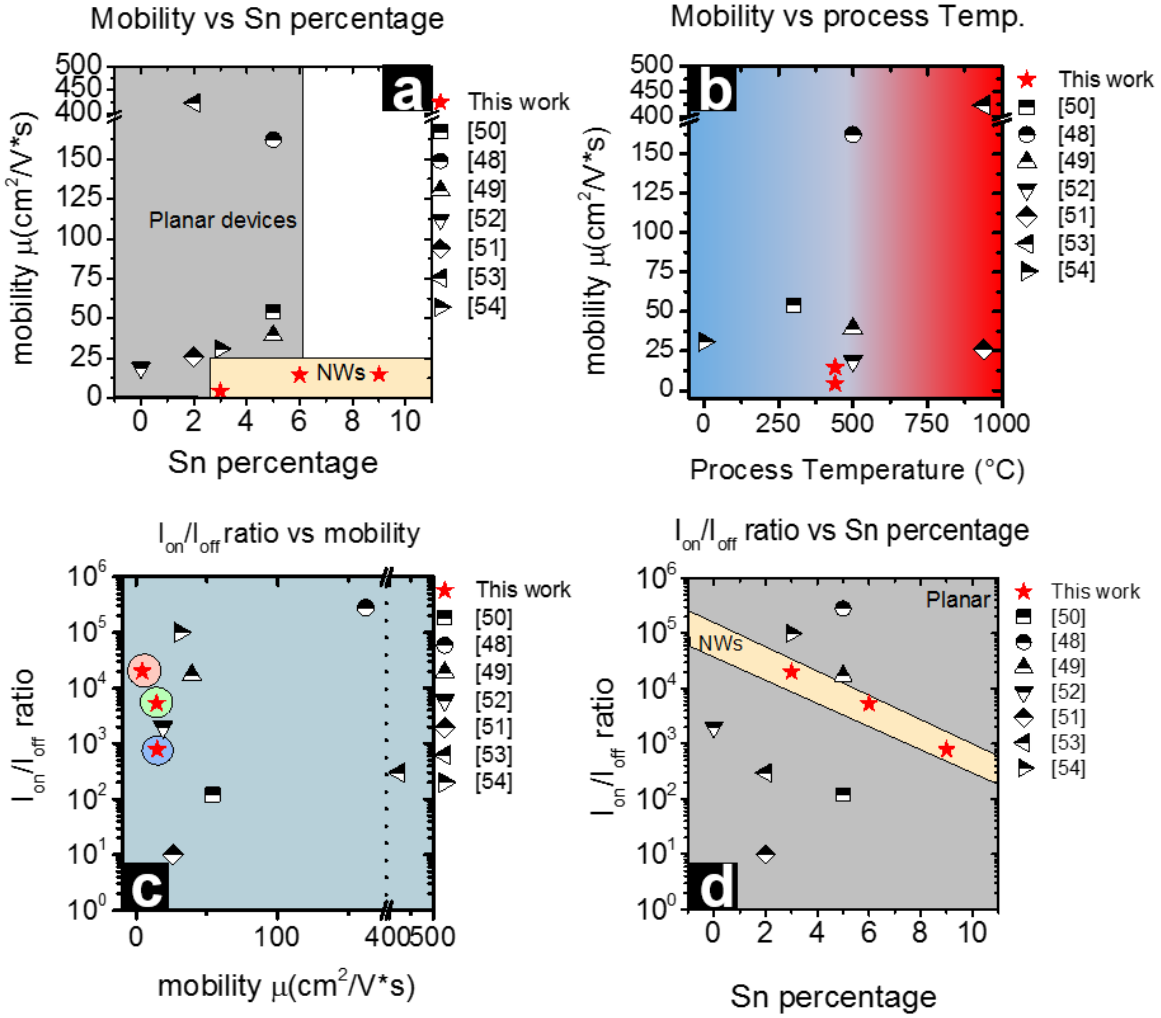

Figure 9: *Electrical parameter comparison with previous works found in literature (a) mobility as a function of different Sn concentration,(b) I_{ON}/I_{OFF} ratio as a function of the process temperature, (c) I_{ON}/I_{OFF} ratio versus mobility for $Ge_{1-x}Sn_x$ nanowires and planar structures, (d) I_{ON}/I_{OFF} ratio as a function of Sn content.*

A concluding remark from this study is that for high speed device applications $Ge_{0.97}Sn_{0.03}$ VLS-grown nanowires appear to be the best material candidate. Nevertheless considering the data variability; as pointed out beforehand; further studies on the surface states and on the metal-semiconductor contacts [55-56] should be addressed in order to reduce the data distribution and to improve the performance of the material that shows high potential for future applications.

IV. CONCLUSIONS

A comprehensive investigation has been made on the electrical performance of $Ge_{0.97}Sn_{0.03}$, $Ge_{0.94}Sn_{0.06}$ and $Ge_{0.91}Sn_{0.09}$ VLS-grown nanowires which were fabricated using a relatively low-temperature process; with a maximum temperature of only 440 °C. From the transfer characteristics, obtained by sweeping the backgate at low V_{ds} voltage, several electrical parameters such as the I_{ON}/I_{OFF} ratio, SS, g_m and mobility were extracted. Comparing the different Sn content in the nanowires it appears that the best electrical performance was obtained for $Ge_{0.97}Sn_{0.03}$ nanowires, due to the intrinsic characteristic of the material. The data extracted in this study represents one of the first in depth electrical investigations of $Ge_{1-x}Sn_x$ nanowires which could potentially be used to calibrate on-going modelling studies, *e.g.* quantisation phenomena as a function of channel length reduction. Finally, in comparing $Ge_{1-x}Sn_x$ device figures of merit, the VLS bottom-up grown have a clear advantage over other fabrication routes, in that the maximum process temperature is only 440 °C, which is relatively low, and thus compatible with back-end-of-line integration schemes in nanoelectronic chip production.

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