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Structural and electrical analysis of the atomic layer deposition of $HfO_2/n\text{-}In_{0.53}Ga_{0.47}As$ capacitors with and without an Al_2O_3 interface control layer

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High mobility III-V substrates with high-*k* oxides are required for device scaling without loss of channel mobility. Interest has focused on the *self-cleaning* effect on selected III-V substrates during atomic layer deposition of Al_2O_3. A thin (~1 nm) Al_2O_3 interface control layer is deposited on $In_{0.53}Ga_{0.47}As$ prior to HfO_2 growth, providing the benefit of *self-cleaning* and improving the interface quality by reducing interface state defect densities by ~50% while maintaining scaling trends. Significant reductions in leakage current density and increased breakdown voltage are found, indicative of a band structure improvement due to the reduction/removal of the $In_{0.53}Ga_{0.47}As$ native oxides. © *2010 American Institute of Physics*. [doi:10.1063/1.3473773]

A critical technological challenge in the integration of high *k*-dielectrics on III-V channels is the control of the high-*k*/III-V interface. Although the interfacial chemistry of the high-*k*/Si system is similar to the SiO_2/Si system,[1] the high-*k*/III-V system is more complex, due to competition between the various native oxide species at the interface,[2] resulting in growth of a poor quality interfacial layer.[3–6] In recent work,[3] reductions in interface state defect densities (D_{it}) were achieved by pre-treatment of the $In_{0.53}Ga_{0.47}As$ surface prior to atomic layer deposition (ALD) of HfO_2 [$k \sim 16–25$, band gap $(E_g) \sim 5.8–6.0$ eV].[7–9] The native oxides of $In_{0.53}Ga_{0.47}As$ (Ga_2O_3, In_2O_3, and As_2O_3) have low band gaps (3.6–4.8 eV) (Refs. 2 and 9) and *k*-values of 8–10 when relating the reported[9,10] *k*-value for Ga_2O_3 and In_2O_3 with the approximate refractive indices ($n \sim 1.9$ for all)[2] through the equation $n^2 \propto k$ and the Moss Inverse Law[11] for the refractive index, *k*-value and energy band gap. They are detrimental to the band structure of high-*k*/III-V devices by increasing the leakage current and creating potential wells in the native oxide layer between the high-*k* oxide and the substrate. The *self-cleaning* Al_2O_3 ALD process is reported to reduce or remove the III-V native oxides.[12–15] However, devices employing Al_2O_3 ($k \sim 8.6–11.6$, $E_g \sim 8.8$ eV) (Refs. 8, 9, and 12) as the gate oxide are limited for scaling due to its low *k*-value.

In this work, the structural and electrical properties of $Pd/HfO_2/n\text{-}In_{0.53}Ga_{0.47}As$ devices (HfO_2: nominal thickness ~3, ~4, and ~5 nm) with/without an ~1 nm Al_2O_3 interface control layer (ICL), are examined using high resolution transmission electron microscopy (HR-TEM) and current/capacitance/conductance versus voltage measurements (JV, CV, and GV, respectively). The devices are labeled: *s*1_3, *s*1_4, *s*1_5 (e.g., sample, ~1 nm Al_2O_3, ~5 nm HfO_2 is labeled *s*1_5). As a control, devices were fabricated without the Al_2O_3 ICL [nominal ~5 nm HfO_2 only (label: *s*0_5)]. The motivation for this work is: (i) to detect any improvement in the quality and structure of the interface using the bilayer approach; (ii) to investigate if an Al_2O_3 ICL improves the electrical performance of devices by modifying the metal-oxide-semiconductor (MOS) band structure; (iii) to determine if scaling is possible with an Al_2O_3 ICL using reducing thicknesses of HfO_2.

The ~2 μm *n*-type (S: $\sim 4 \times 10^{17}$ cm^{-3}) $In_{0.53}Ga_{0.47}As$ channels had a ~0.1 μm InP buffer layer (S: $\sim 2 \times 10^{18}$ cm^{-3}) on a ~350 μm InP substrate (S: $3–8 \times 10^{18}$ cm^{-3}). All $In_{0.53}Ga_{0.47}As$ layers were grown by MOVPE. An *ex situ* three-stage surface pre-treatment process [HCl, NH_4OH, and $(NH_4)_2S$] was performed on the $n\text{-}In_{0.53}Ga_{0.47}As$/InP substrates which has previously been shown to be beneficial to device performance.[3] The Al_2O_3 and HfO_2 layers were deposited in a Cambridge NanoTech Fiji F200LLC ALD system, at 250 °C. The ALD of Al_2O_3 and HfO_2 employed alternating pulses of TMA $[Al(CH_3)_3]/H_2O$ and tetrakis(ethylmethylamino)hafnium (TEMAH) $\{Hf[N(C_2H_5)(CH_3)]_4\}/H_2O$, respectively. MOS structures were completed by vacuum evaporation of ~200 nm of Pd at a deposition rate of 2.5 Å/s using a lift-off process. No ohmic back contacts were formed.

Figures 1(a) and 1(b) present cross-sectional HR-TEM micrographs of *s*1_5 and *s*0_5, confirming the physical oxide and nominal thicknesses are in close agreement: *s*1_5 [Fig. 1(a)] has a ~5.3 nm HfO_2 layer, and a ~1.2 nm Al_2O_3 layer. *s*0_5 [Fig. 1(b)], has a ~4.9 nm HfO_2 layer. All oxide layers are amorphous. Comparison between Figs. 1(a) and 1(b) shows a ~0.7 nm native oxide layer at the high-*k*/$n\text{-}In_{0.53}Ga_{0.47}As$ interface when no Al_2O_3 ICL is deposited, which is indicative of an Al_2O_3 *self-cleaning* effect on the native oxide, for sample *s*1_5.

Figure 2(a) presents a cross-sectional HR-TEM micrograph of *s*1_3. The physical thicknesses of HfO_2 and Al_2O_3 are ~3.2 nm and ~1.2 nm, respectively. Figure 2(b), a plan-view HR-TEM micrograph for sample *s*1_5, reveals the epitaxial 2 μm $n\text{-}In_{0.53}Ga_{0.47}As$ layer to be defect-free,

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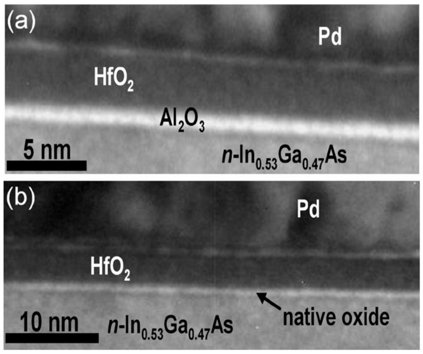

FIG. 1. Cross-sectional HR-TEM micrographs of (a) $s1\_5$, with $\sim$5.3 nm HfO_2 and $\sim$1.1 nm Al_2O_3 and (b) $s0\_5$, with $\sim$4.9 nm HfO_2 and a $\sim$0.7 nm native oxide layer.

with an associated negligible root mean square (rms) surface roughness of <1 nm.

Figure 3 shows (a) JV responses and (b) the measured 1 kHz CV responses, along with the simulated[16] CV curves for all samples. The inset to Fig. 3(a) shows the capacitance equivalent thickness (CET) versus HR-TEM extracted HfO_2 physical thickness plot for the bilayer sample set ($s1\_3, s1\_4, s1\_5$), with a linear fit. Figure 3(a), when assessing the bilayer sample set only, shows that leakage current density increases with reducing HfO_2 thickness, and the dielectric breakdown voltage increases with increasing HfO_2 thickness. This is expected for a dominant quantum-mechanical (QM) tunneling leakage mechanism with similar energy barrier height and shape, and for a dominant electrically-controlled oxide breakdown process.[17] However, the leakage current density response for sample $s0\_5$ is substantially higher (approximately three orders of magnitude at 3 V) than for sample $s1\_5$, showing that the absence of an Al_2O_3 ICL changes the tunneling barrier height/shape to conduction beyond a thickness-dependency regime only and introduces an additional, highly temperature-dependent (not shown), trap-assisted conduction mechanism that adds magnitude and fluctuation to the response.[18] Figure 3(b) shows that the accumulation maximum capacitance at 2 V scales correctly with oxide thickness for the bilayer sample set. The simulated curves confirm that surface accumulation is achieved at 2 V for all samples.[3] The accumulation maximum capacitance is greater for the measured data compared to the simulated data, showing the existence of a QM correction factor. This difference could be due to additional states inside the conduction band at the oxide/n-$In_{0.53}Ga_{0.47}As$ interface,[19] and/or charge quantization leading to X and L satellite valley occupation in the conduction band.[20] We see a similar maximum accumulation capacitance for the $\sim$5 nm HfO_2 samples with/without Al_2O_3 ($s1\_5$ and $s0\_5$, respectively), showing that the overall equivalent oxide thickness of these oxide stacks are similar. The observed variation in the maximum accumulation capacitance ($\sim$0.003 F/m^2) for sample $s0\_5$ is likely due to native oxide layer thickness variation not observable by HR-TEM. Given the large difference in leakage current density between these samples ($s1\_5$ and $s0\_5$), it is evident that the Al_2O_3 ICL substantially reduces the native oxide layer thickness while increasing the barrier height to electron tunneling from the $In_{0.53}Ga_{0.47}As$ conduction band. The linear fit of the inset to Fig. 3(a) shows that the reduction in HfO_2 thickness for the bilayer structures produces the required scaling trend. This linear fit can be used to extract an intercept CET value, which has contributions from Al_2O_3, any underlying native oxide layer (if present), and the QM correction contribution from the n-$In_{0.53}Ga_{0.47}As$ accumulation layer. HR-TEM [Figs. 1(a), 1(b), and 2(a)], in combination with the electrical results [Figs. 3(a), 3(b), 4(a), and 4(b)], indicate that no substantive underlying native oxide layer is present for the bilayer sample set. Assuming this is the case and since we can extract the contributions from Al_2O_3, we can thereby determine a QM correction factor of $\sim$0.7 nm. From the slope of the linear fit we can estimate the HfO_2 k-value to be $\sim$20, which is within the reported range.[7] Reasonable assumptions used were: (i) the k-value of both Al_2O_3 and any native oxide[2,10,12] layer is $\sim$9 and (ii) the physical thicknesses used for sample $s1\_4$ are nominal thicknesses proportionally corrected using HR-TEM/nominal-thickness ratios and ALD cycle ratios for other samples. The absence of an underlying native oxide

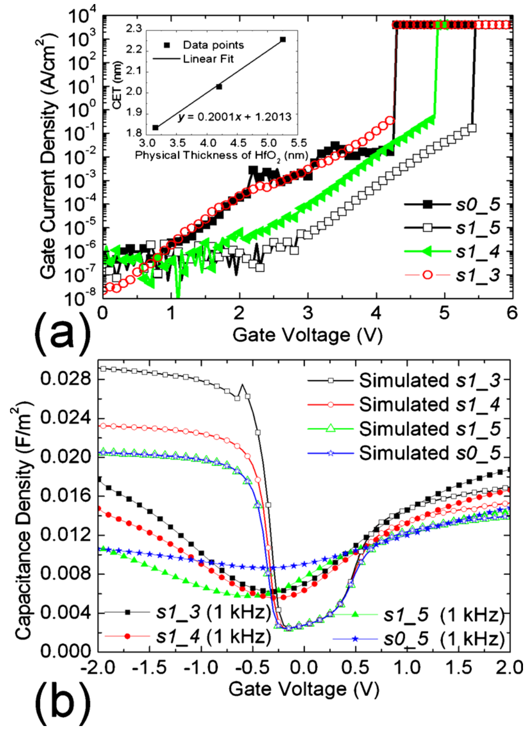

FIG. 3. (Color online) (a) JV responses for all samples, with significantly lower leakage for the $s1\_5$ (Al_2O_3 ICL) devices, compared to $s0\_5$ devices. (b) Measured and simulated (from the 1D Poisson–Schrödinger solver) 1 kHz CV responses for all samples. Inset to (a) shows the CET vs physical thickness with a linear fit.

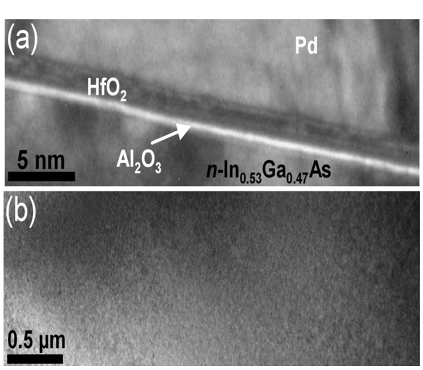

FIG. 2. HR-TEM micrographs of (a) $s1\_3$ (cross-sectional), with $\sim$3.2 nm HfO_2 and $\sim$1.2 nm Al_2O_3; (b) $s1\_5$ (plan-view) shows a defect free n-$In_{0.53}Ga_{0.47}As$ substrate layer.

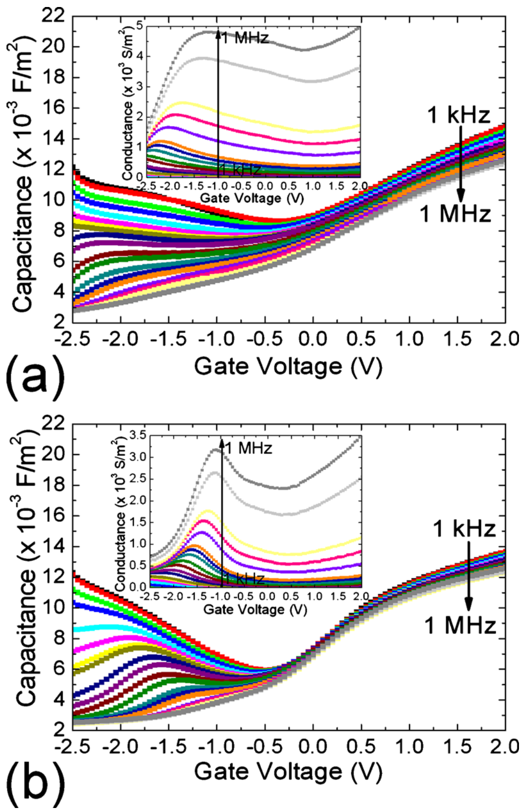

FIG. 4. (Color online) (a) and (b) show CV responses (20 frequencies; 1 kHz–1 MHz) for samples $s0\_5$ and $s1\_5$, respectively. The insets to (a) and (b) show the corresponding GV responses.

layer, evidenced by HR-TEM in combination with the electrical results, indicates that the Al_2O_3 is likely to be removing the native oxides via the *self-cleaning* process.

Figures 4(a) and 4(b) show the multifrequency CV responses for samples $s0\_5$ and $s1\_5$, respectively. The insets to Figs. 4(a) and 4(b) show the corresponding GV responses. We observe an increased D_{it} response in both the CV and GV profiles for sample $s0\_5$ when compared to the equivalent response for sample $s1\_5$, which includes (over the entire voltage range) an increased CV and GV stretch-out and frequency dispersion. In the voltage range -1 to 0.25 V, the absence of minority carriers is assumed, corresponding to the depletion regime. An approximation to the Conductance Method[21] indicates that samples $s0\_5$ and $s1\_5$ have estimated D_{it} values of $\sim 8\times 10^{12}$ cm^{-2} eV^{-1} and $\sim 4\times 10^{12}$ cm^{-2} eV^{-1}, respectively. Due to the absence of distinct equivalent parallel conductance (G_p/ω) peaks as observed in SiO_2/Si systems, this is derived assuming zero standard deviation in band bending using values of G_p/ω at -1 V and taken at 30 kHz. While it is noted that the G_p/ω magnitudes may be affected by the approximation conditions, and any possible minority carrier contribution, the relative difference provides a valid estimate. There is approximately a 50% reduction in D_{it} when including an Al_2O_3 ICL.

In summary, it is found that the inclusion of a thin Al_2O_3 ICL ($\sim$1 nm) at the $HfO_2/In_{0.53}Ga_{0.47}As$ interface improves the structural and electrical properties of Pd/HfO_2/n-$In_{0.53}Ga_{0.47}As$ devices. The inclusion of the Al_2O_3 ICL improves the breakdown voltage and reduces leakage current densities by approximately three orders of magnitude at 3 V by increasing the barrier height to tunneling from the $In_{0.53}Ga_{0.47}As$ conduction band into the oxide. No apparent native oxide layer is observed at the high-k/$In_{0.53}Ga_{0.47}As$ interface when using an Al_2O_3 ICL, suggesting that the Al_2O_3 ALD process is *self-cleaning* the $In_{0.53}Ga_{0.47}As$ native oxides. Comparing the electrical performance for the bilayer samples with different HfO_2 thicknesses we find that device scaling trends can be achieved. Combining the structural and electrical results we find a QM correction factor of $\sim$0.7 nm. The inclusion of an ICL causes an approximate 50% reduction in D_{it}, thereby improving the quality of the interface.

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